

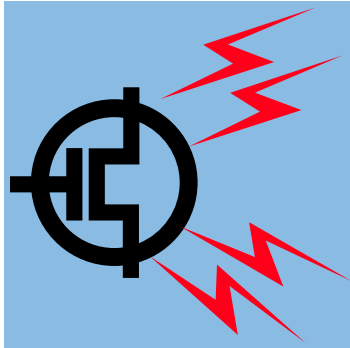
GETTING IT RIGHT

COLLABORATING FOR MISSION SUCCESS

VOLUME 10 | ISSUE 3 | MARCH 2020

WORKSHOP COVERS LATEST IN MICROELECTRONICS

By ADAM BUSHMAKER
The Aerospace Corporation



The Microelectronics Reliability & Qualification Workshop (MRQW) provided a forum for open discussion of issues for microelectronics targeted for use in space systems. The 2020 meeting consisted of 3 days with 60 speakers in multiple technical sessions.

Invited speakers covered the latest technology and work in progress in different areas of microelectronics device reliability and qualification methodologies, including:

- advanced technologies reliability issues
- advanced space FPGAs and memories
- RF, analog, and mixed-signal device and design issues
- space radiation effects
- reliability for extreme environments
- advanced packaging issues
- failure analysis
- GaN reliability and radiation effects
- emerging technologies
- alternate grade parts
- trust and verification science

Highlights from 2020 MRQW included a session on the ongoing work of the High Reliability Electronics Virtual program.

Current and past MRQW proceedings

are available on the event website: <https://aerospace.org/MRQW/>.

For more information, contact Adam Bushmaker, 310.336.7513, adam.w.bushmaker@aero.org.



Keynote speaker, Dr. John Cressler (L), Schlumberger Chair Professor from Georgia Tech, presented the first practical bandgap-engineered device to be successfully implemented in silicon. Keynote speaker, Dr. David Miller (R), Chief Technology Officer for The Aerospace Corporation, described three micro-gravity technology research facilities to mature dynamics and control technology.

THE SiGe HBT DREAM

By JOHN D. CRESSLER
Georgia Institute of Technology,
Atlanta, GA

Microelectronic device and circuit designers have long sought to combine the superior transport properties and design flexibility offered by bandgap engineering (as routinely practiced in compound semiconductors such as gallium arsenide and indium phosphide), with the high yield and low cost of conventional silicon (Si) fabrication. With the introduction of epitaxial silicon germanium (SiGe) alloys, that dream has finally become a reality.

The SiGe heterojunction bipolar transistor (HBT) is the first practical bandgap-engineered device to be realized in the silicon material system. Integration of SiGe HBTs with

best-of-breed Si complementary metal oxide semiconductors (CMOS) to form a SiGe HBT BiCMOS technology is an obvious fit for addressing emerging system-on-

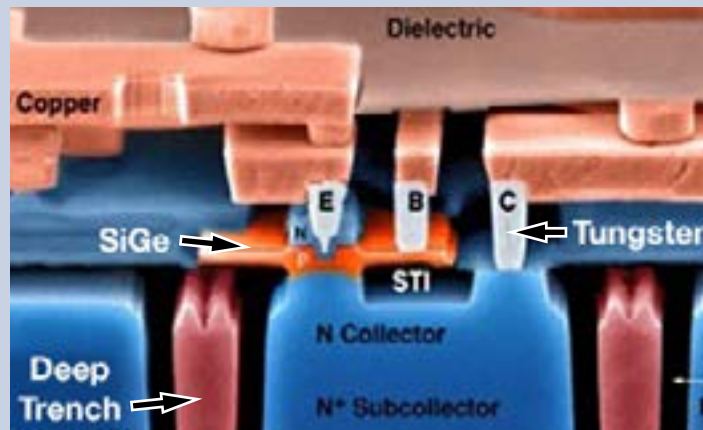
a-chip and system-on-a-package integrated circuit solutions.

While SiGe technology enjoys a growing importance in performance-constrained analog, digital, and radio frequency through mm-wave circuits and systems, emerging

SiGe applications for which reliability issues present both nuanced challenges and exciting opportunities include space systems, the quantum realm, power electronics, and integrated photonics.

The notion of integrated circuit reliability must be broadened beyond classical interpretation to address:

- robust operation from direct current to near-Tera Hz speeds, under both static and dynamic electrical stress, as a function varying impedance environments and feedback mechanisms
- operation over extreme temperatures
- operation within intense radiation fields, including total ionizing dose, displacement damage, and single event transient phenomena



Scanning electron micrograph of a SiGe HBT. The SiGe alloy is shown in orange. Photo courtesy of John D. Cressler

For more information, contact John D. Cressler, 404.894.5161, cressler@ece.gatech.edu.

INCREASING MICROCIRCUIT/HYBRID PROBLEMS

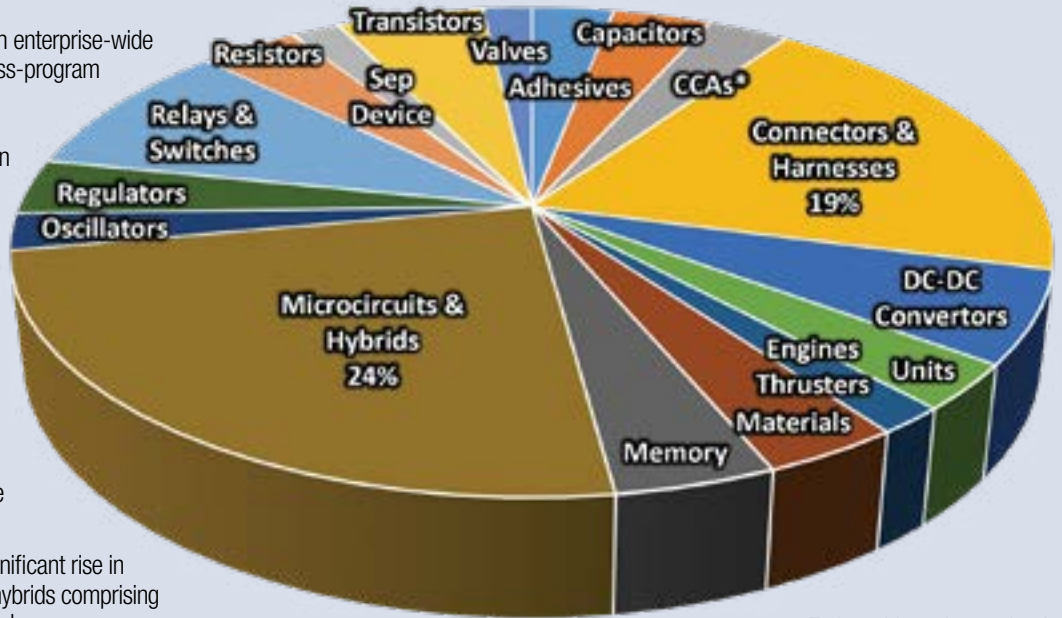
By WILLIAM McKEITHAN
The Aerospace Corporation

The Aerospace Corporation administers an enterprise-wide information sharing process to enable cross-program early problem alerts for our government customers. Timely dissemination of failure data and related reports ensures mitigation of emerging problems. Early alerts assist programs in improving the availability, reliability, maintainability, quality, and safety of their systems. Addressing potential issues and risks before they are realized problems has the added benefit of reducing overall system costs.

The alert system is a compilation of government, industry, and internally generated emerging issues. Historically, harnesses and connectors have been the category of greatest concern.

In the past two years there has been a significant rise in issues associated with microcircuits and hybrids comprising more than 24% of all the early alerts issued.

Identification of issues and/or obvious trends in the supply chain is the first step to developing risk mitigation strategies during design and manufacturing to ensure delivery of reliable space systems.



Early problem alerts calendar years 2018–2019 binned by part type.

*Circuit Card Assemblies

For more information, contact Bill McKeithan, 571.304.7839, william.w.mckeithan@aero.org.

HiRev TECHNOLOGY FORECAST

By JAMES JOHANSEN
The Aerospace Corporation

Market dynamics in the microelectronics industrial base are so volatile that even within a few months information that was late-breaking news is overcome by new developments.

Five noteworthy areas of development include:

- government investments
- major industry developments
- government policy engagement on areas including trust
- government technology engagements and maturation
- government-owned fabrication source developments

The U.S. government continues to ensure fabrication capabilities exist for strategic chip manufacturing needs across the board. There is a dependence on key integrated circuits for several systems, so monitoring of microelectronics developments continues to seek, adapt, and devise resilient and cost-effective methods to maintain critical parts needs.

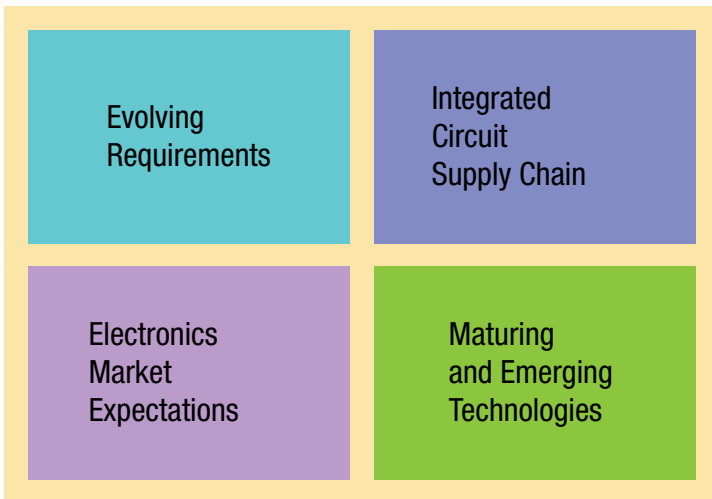
Additional funding will likely be required for development of alternative domestic suppliers and evaluations of the use of alternate-grade parts such as avionics-grade, automotive, and commercial parts with the associated

risks for radiation and non-trust. Ensuring microelectronic foundries of last resort and maintaining critical capabilities for future systems are part of the trade space.

As a part of the HiRev (High Reliability Electronics Virtual) program, The Aerospace Corporation, working with the Air Force Research Laboratories and Defense Microelectronics Activity, has collected trending data and developed a range of mitigation options with future possible contingencies. Trends and technology forecast results for digital, analog, mixed signals, and power components are detailed in a recently published report.¹

For more information, contact James Johansen, 310.336.0779, james.d.johansen@aero.org.

¹ TOR-2019-01585, HiRev 2019 Microelectronic Technology Forecast with a Focus on Space Applications Needs, September 17, 2019



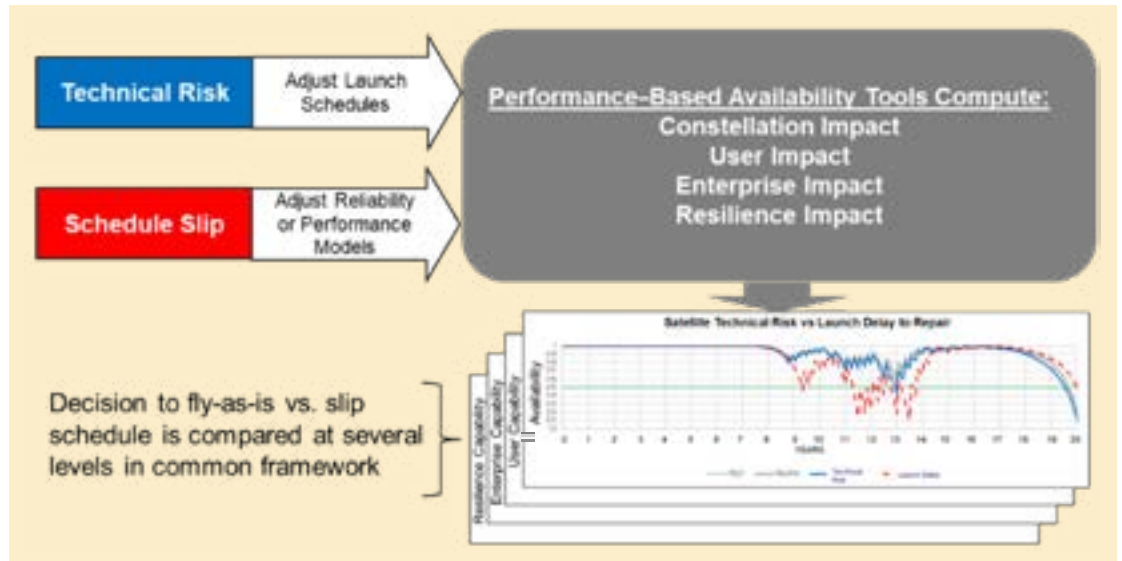
Dynamic and rapidly evolving landscapes present new challenges and opportunities for high-reliability assurance that requires tracking for future trends.

BALANCING RISK AND SCHEDULE

By JAMES WOMACK
The Aerospace Corporation

Technical risk is traditionally assessed based on mission impact to an individual satellite and the likelihood of occurrence. A separate analysis is required to determine the delays and additional costs to mitigate the technical risk. Tradeoffs to delay or to launch a satellite with technical risk can be difficult and usually do not include long-term impacts to the constellation or enterprise. They don't provide a method to directly measure the differences between fly-as-is versus slipping the schedule to repair. A method was developed to make direct comparisons between the impacts to either accept the technical risk or slip the schedule.

The likelihood of reduced performance is modeled using multistate satellite reliability models that include all possible satellite performance states, and impacts are determined by the constellation performance models. Satellite failure risk is evaluated in performance-based functional availability (PFA) tools by modifications to the satellite reliability models. These models can address risks at the piece-part level, such as suspect microelectronics as a function of reduced performance and likelihood of occurrence. Schedule slips are incorporated into



PFA tools by adjusting the scheduled satellite launch times. Models for ground segments, external threats, and mitigations are also included in PFA tools.

PFA plots overlay the impacts from technical risk and schedule slips at the constellation, user, enterprise, and resilience levels. The constellation impacts are shown as future availability and other impacts are shown as distributions of key constellation future performance metrics. Resilience impacts are computed under the assumption of one or more external probabilistic threats and mitigations. Once a PFA tool is established for a constellation, regenerating impact plots is quickly accomplished for any given technical risk or schedule slips allowing for direct comparisons at multiple impact levels.

For more information, contact James Womack, 310.336.7647, james.m.womack@aero.org.

OPTIMIZING ELECTRONICS TEST/ANALYSIS RATIO

By CHARLES HYMOWITZ
AEI Systems, LLC

Test and analysis can assess electronics reliability, but budget and time constrained programs often shun analysis as too expensive or challenging. In many cases, little to no analysis is performed. But is testing alone more cost effective in

improving reliability?

Test tells us what is. Test has many potential pitfalls: bad data, bad equipment, and bad interpretation. Test determines typical performance and requires parts to be produced prior to build. Test alone can miss specified requirements for beginning or end-of-life, overlook derived

requirements, and is only valid for the measurement lot.

Analysis tells us what it could be. Analysis computes margins, risk, parameter sensitivity, and identifies fatal and rare events. Performance aspects are examined, quantified, and evaluated through a series of analyses (worst-case circuit analysis, stress

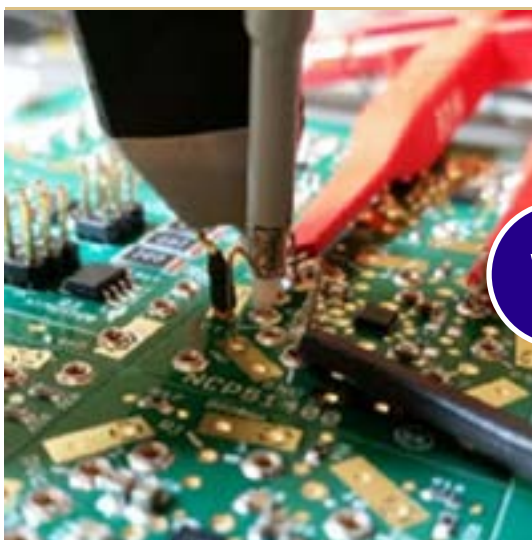
and derating, failure mode, effects and criticality analysis, and mean time between failures).

Analysis should target tolerance ratios, heritage reference designs, and stress levels combined with failure modes analysis. Analysis problem discovery is in the derived requirements, minor design changes, signal integrity-power integrity, and at the interfaces/connectors.

Checklists exist with guidelines for selected applications based on historical use and current needs! Analysis can gain confidence from nominal performance and limited statistical test data. Test and analysis make for a powerful combination if applied complementarily even when constrained.

Go to aeng.com for more information, or contact Charles Hymowitz, 310.216.1144, charles@aeng.com.

1TOR-2012(8960)-4 REV A—Electrical Design Worst-Case Circuit Analysis Guidelines and Draft Standard



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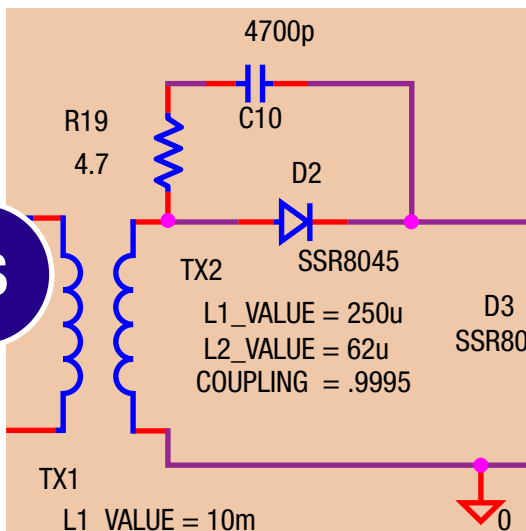


Photo courtesy of Picotest.com and AEI Systems, LLC

UNIVERSITY STUDENTS DEVELOP RADIATION TEST FIXTURE

By ALLYSON YARBROUGH
and JOHN SCARPULLA
The Aerospace Corporation

BRYAN SMITH, EDGAR PALAPA,
HUGO MORALES, LUIS TEPOX, and
MARVIN SOLTERO
College of Engineering,
Computer Science and Technology,
California State University,
Los Angeles



Project team members from left to right: Bryan Smith, Edgar Palapa, Hugo Morales, Luis Tepox, and Marvin Soltero.

Photography courtesy of Benjamin V. Campos. Jr.

Commercial off-the-shelf electronics are often used in small satellites for their advanced capabilities, low procurement cost, and short lead times. The electronics' sensitivity to the natural space radiation environment is an important use factor.

Radiation testing is needed, but affordable evaluation boards are frequently not available from the vendors. Users must design a costly custom test board for each device to monitor performance during test.

The Senior Capstone Project is a partnership between The Aerospace Corporation and California State University, Los Angeles. Five graduating seniors were selected to

develop a mixed-signal test fixture with the following requirements:

- accommodate devices such as analog-to-digital converters
- provide remote control operation for use outside laboratory radiation sources at distances up to 100 ft. cable lengths. The team has selected the Texas Instruments™ digital-to-analog converter DAC7311 as an example test device. The brassboard test fixture and software scripts are completed

and the radiation tests are planned for Spring 2020

The project should result in a low-cost, adaptable, general-purpose hardware/software test platform that can accommodate multiple electronic device types during radiation testing.

For more information, contact Allyson Yarbrough, 310.336.1499, Allyson.D.Yarbrough@aero.org, or John Scarpulla, 310.336.7998, John.R.Scarpulla@aero.org.

2020 EVENTS

March 2–5 *Ground System Architectures Workshop (GSAW), Los Angeles, CA*

March 7–14 *2020 IEEE Aerospace Conference, Big Sky, MT*

March 24–25 *Spacecraft Thermal Control Workshop (STCW), Torrance, CA*

March 31–April 2 *32nd Aerospace Testing Seminar (ATS), Los Angeles, CA*

April 20–23 *Space Power Workshop (SPW), Torrance, CA*

April 21–22 *AIAA SOSTC Improving Space Operations Workshop 2020, Suitland, MD*

May 5–6 *Space Parts Working Group (SPWG), Torrance, CA*

May 5–7 *Systems Engineering Forum, Model Based Systems Engineering, Chantilly, VA*

May 5–7 *AIAA Defense and Security Forum (AIAA DEFENSE Forum), Laurel, MD*

May 8 *Trusted Autonomous Systems (ITAR-Restricted Course), Laurel, MD*

May 13–15 *45th Aerospace Mechanisms Symposium, Houston, TX*

May 27–28 *Advancing Cybersecurity Risk Management Conference, Gaithersburg, MD*

June 2–4 *Spacecraft and Launch Vehicle Dynamic Environments Workshop, El Segundo, CA*

July 20–24 *IEEE Nuclear and Space Radiation Effects Conference (NSREC), Santa Fe, NM*



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Getting It Right is published every three months by the Corporate Chief Engineer's Office within the Office of the Executive Vice President of The Aerospace Corporation. Direct questions and comments to gettingitright@aero.org.

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RECENT GUIDANCE AND RELATED MEDIA

Developing a Sustainable Spectrum Approach to Deliver 5G Services and Critical Weather Forecasts by D.G. Lubar et al.; OTR202000209; PR

Large Constellation Disposal Hazards by W.H. Ailor; OTR201901097; PR

Application and Tailoring Guidance for Standards Used on Space System Acquisitions by B.E. Shaw; TOR-2019-02267; USGC

U.S. Space Program Mission Assurance Summit, November 12-13, 2019 by G. Johnson-Roth; TOR-2020-00276; USGC

2019 Satellite Lifetime Study—Executive Summary by K. Ferrone et al.; TOR-2020-00386; PR

Interface Modelling and Evaluation with Multiple Model-Based Systems Engineering Tools by R.B. Crombie et al.; ATR-2019-02460; USGC

Small Satellite Cost Model 2019 (SSCM19) User's Manual by E.A. Mahr; ATR-2019-02492-Rev A; USGC

Model Based Systems Engineering (MBSE) Strategy Workshops by A.C. Hoheb et al.; ATR-2020-00036; USGC

Space Collaboration Council—November 12, 2019 by T. Tran et al.; ATR-2020-00418; USGC

Evaluating the Impact of Autonomy on Future Ground & Space Systems by C.M. Lawson; TOR-2019-02622; USGC

Modular Spacecraft Buses—Design Evolution and Current Capabilities by M.N. Tran; TOR-2019-02746; USGC

Model-Based RFPs Depend on Defined Program Objectives by A.C. Hoheb; ATR-2020-00181; USGC

PR = Approved for public release
USGC = Approved for release to U.S. government agencies and their contractors
USG = Approved for release to U.S. government agencies

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